



Ultra-Energy-Efficient Machine Learning Hardware: Microwatt Biomedical Processor and In-Memory Computing Designs

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Abstract

In recent years, deep learning algorithms have been widespread across many practical applications. Algorithms trained by offline back propagation using pre-defined datasets show impressive performance, but state-of-the-art algorithms are compute-/memory-intensive, making it difficult to perform low-power real-time classification with low energy consumption on embedded hardware platforms.

This is especially true for wearable devices that exhibit very stringent power and area constraints. Targeting a smart security engine on wearable devices, I will first present a 1 μ W ECG ASIC processor with highly compressed neural networks, which demonstrates ECG-based authentication on a >600-subject database.

Next, I will discuss our recent research works on “*in-memory computing*” (analog computation along bitline with all rows asserted) for deep learning systems, which is a promising technique to achieve large energy gains over all-digital ASIC. We have designed new bitcells and macros for in-memory computing based on both SRAM (65nm) and RRAM (monolithic integration with 90nm CMOS) and fabricated prototype chips. Compared to row-by-row sequential designs, our SRAM and RRAM in-memory computing prototype chips show >30X energy improvement on MAC and convolution operations, while maintaining >85% accuracy on CIFAR-10 dataset.

Biography

Jae-sun Seo received his Ph.D. degree from University of Michigan in 2010. From 2010 to 2013, he was with IBM T. J. Watson Research Center, where he worked on energy-efficient circuits for microprocessors and cognitive computing chip design for the DARPA SyNAPSE project. In January 2014, he joined Arizona State University as an assistant professor in the School of ECEE. His research interests include efficient hardware design for deep learning and neuromorphic computing, as well as integrated power management. During the summer of 2015, he was a visiting faculty at Intel Circuits Research Lab. He was a recipient of IBM Outstanding Technical Achievement Award in 2012 and NSF CAREER Award in 2017.

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